CLAIMS:

1. A burst receiver for delivering to a media access controller (MAC) radio frequency TDMA signal bursts transmitted on an upstream channel of a cable transmission system, the receiver comprising:

an input circuit connected to the upstream channel;

a symbol clock operating at a given symbol rate;

a signal path from the input circuit to the MAC, the signal path carrying a data representative signal at the given symbol rate;

an open loop resampler in the signal path for sampling the data representative signal at the given symbol rate; and

a closed loop resampler in the signal path for adjusting the phase of the symbol clock to match the data representative signal.

2. The burst receiver of claim 1, in which the input circuit includes a frequency down-converter.

3. The burst receiver of claim 2, in which the frequency down-converter includes a direct digital frequency synthesizer and a mixer having two inputs, the upstream channel being coupled to one input of the mixer and the frequency synthesizer being coupled to the other input of the mixer.

4. The burst receiver of claim 3, in which the input circuit additionally comprises an analog-to-digital converter.

5. The burst receiver of claim 1, additionally comprising a matched filter coupling the open loop resampler to the closed loop resampler such that the matched filter precedes the closed loop.

6. The burst receiver of claim 2, in which the data representative signal is a preamble.

7. The burst receiver of claim 2, in which the data representative signal is a payload.

8. The burst receiver of claim 2, in which the data representative signal is a preamble and a payload.

9. The burst receiver of claim 1, in which the symbol clock has two differently phased outputs, and the closed loop resampler samples the data representative signal responsive to both outputs of the symbol clock, determines the phase difference between both output samples and the symbol clock, and adjusts the phase of the symbol clock responsive to the smaller difference.

10. The burst receiver of claim 6,in which the two outputs of the symbol clock are 180 degrees out of phase with each other.

11. The burst receiver of claim 1, in which the closed loop resampler comprises: a phase detector having a first input to which the data representative signal is applied, a second input to which the output of the symbol clock is applied, and an output; a loop filter connected between the output of the phase detector and the symbol clock to smooth the phase adjustments made by the phase detector to the symbol clock; and a gain control circuit that monitors the amplitude of the data representative signal and modifies the output of the phase detector before it is applied to the loop filter depending on the amplitude of the data representative signal.

12. The burst receiver of claim 11, in which the loop filter has coefficients designed for a particular range of amplitude

variation and the gain control circuit modifies the output of the phase detector to keep said output within the particular range.

13. The burst receiver of claim 1, additionally comprising a demodulator in the signal path for converting the data representative signal to binary data and counters for recording statistics relating to traffic on the system, the signal path carrying both the binary data and data representing the counter states to the MAC.

14. The burst receiver of claim 13, in which the MAC generates for downstream transmission MAP messages that identify cable modems, specify time slots assigned to the identified cable modems, and describe burst configurations to be transmitted upstream in the specified time slots, the MAC transmits the MAP messages to the demodulator and the demodulator uses the burst configurations to convert the data representative signal to binary data.

15. The burst receiver of claim 14, in which the MAC stores the MAP messages and transmits the individual MAP messages to the demodulator in real time during the specified time slots.

16. The burst receiver of claim 15, in which the MAC filters the MAP messages before transmission to the burst receiver to eliminate some of the information contained in the MAP messages.

17. The burst receiver of claim 16, in which the MAC retains an SID, an IUC, and a time slot length of each MAP message during filtering for storage.

18. The burst receiver of claim 1, in which the burst receiver has a plurality of burst configuration registers that store data packet characteristics depending on an IUC.

19. The burst receiver of claim 1, additionally comprising a demodulator in the signal path for converting the data representative signal to binary data and a source of control information, the signal path carrying both the binary data and the control information to the MAC in band such that the control information is appended to the binary data.

20. The burst receiver of claim 19, in which the appended control information is encapsulated with a header to distinguish the control information from the binary data.

21. The burst receiver of claim 19, in which the appended control information comprises an identifier of a cable modem.

22. The burst receiver of claim 19, in which the burst receiver generates channel statistics and the appended control information comprises the generated channel statistics.

23. The burst receiver of claim 19, in which the burst receiver generates ranging offsets and the appended control information comprises the generated ranging offsets.

24. The burst receiver of claim 19, in which the appended control information includes the mode of upstream data transmission.

25. The burst receiver of claim 19, in which the appended control information includes an interval usage code.

26. The burst receiver of claim 19, in which the appended control information includes equalizer coefficients.

27. The burst receiver of claim 1, additionally comprising a plurality of data storage registers in the MAC for storing different burst configurations that depend on the slot type, a burst configuration register in the demodulator, and a multiplexer coupling the data storage registers in the MAC to the burst configuration register in the demodulator to selectively transfer the contents of one of the data storage registers to the burst configuration register depending on the slot type.

28. A receiver that receives a signal transmitted through a cable transmission system, comprising:

an analog to digital converter;

a matched filter coupled to said analog to digital converter; and,

a closed loop resampler coupled to said matched filter.

29. The burst receiver of claim 28, in which the matched filter is coupled to the analog to digital converter by a frequency down-converter.

30. The burst receiver of claim 29, in which the frequency down-converter includes a direct digital frequency synthesizer and a mixer having two inputs, the analog to digital converter being coupled to one input of the mixer and the frequency synthesizer being coupled to the other input of the mixer.

31. The burst receiver of claim 30, additionally comprising an open loop resampler connected between the analog to digital converter and the matched filter.

32. The burst receiver of claim 31, in which the closed loop resampler has a symbol clock with two differently phased outputs, and the closed loop resampler samples the signal responsive to both outputs of the symbol clock, determines the phase difference between both output samples and the symbol clock, and adjusts the phase of the symbol clock responsive to the smaller difference.

33. The burst receiver of claim 32,in which the two outputs of the symbol clock are 180 degrees out of phase with each other.

34. The burst receiver of claim 33, in which the closed loop resampler comprises a phase detector having a first input to which the signal is applied, a second input to which the output of the symbol clock is applied, and an output; a loop filter connected between the output of the phase detector and the symbol clock to smooth the phase adjustments made by the phase detector to the symbol clock; and a gain control circuit that monitors the amplitude of the signal and modifies the output of the phase detector before it is applied to the loop filter depending on the amplitude of the data representative signal.

35. The burst receiver of claim 34, in which the loop filter has coefficients designed for a particular range of amplitude variation and the gain control circuit modifies the output of the phase detector to keep said output within the particular range.

36. The burst receiver of claim 35, additionally comprising a demodulator for converting the signal to binary data, counters for recording statistics relating to traffic on the system, a MAC, and a signal path from the demodulator to the MAC for carrying both the binary data and data representing the counter states to the MAC.

37. The burst receiver of claim 36, in which the MAC generates for downstream transmission MAP messages that identify cable modems, specify time slots assigned to the identified cable modems, and describe burst configurations to be transmitted upstream in the specified time slots, the MAC transmits the MAP messages to the demodulator and the demodulator uses the burst configurations to convert the data representative signal to binary data.

38. The burst receiver of claim 37, in which the MAC stores the MAP messages and transmits the individual MAP messages to the demodulator in real time during the specified time slots.

39. The burst receiver of claim 38, in which the MAC filters the MAP messages before transmission to the burst receiver to eliminate some of the information contained in the MAP messages.

40. The burst receiver of claim 39, in which the MAC retains an SID, an IUC, and a time slot length of each MAP message during filtering for storage.

41. The burst receiver of claim 40, in which the burst receiver has a plurality of burst configuration registers that store data packet characteristics depending on the IUC.

42. The burst receiver of claim 28, additionally comprising a demodulator for converting the signal to binary data, a source of control information, and a MAC for receiving both the binary data and the control information in band such that the control information is appended to the binary data.

43. The burst receiver of claim 42, in which the appended control information is encapsulated within a header to distinguish

the control information from the binary data.

44. The burst receiver of claim 43, in which the appended control information comprises an identifier of a cable modem.

45. The burst receiver of claim 43, in which the burst receiver generates channel statistics and the appended control information comprises the generated channel statistics.

46. The burst receiver of claim 43, in which the burst receiver generates ranging offsets and the appended control information comprises the generated ranging offsets.

47. The burst receiver of claim 43, in which the appended control information includes the mode of upstream data transmission.

48. The burst receiver of claim 43, in which the appended control information includes an interval usage code.

49. The burst receiver of claim 43, in which the appended control information includes equalizer coefficients.

50. The burst receiver of claim 42, additionally comprising a plurality of data storage registers in the MAC for storing different burst configurations that depend on the slot type, a burst configuration register in the demodulator, and a multiplexer coupling the data storage registers in the MAC to the burst configuration register in the demodulator to selectively transfer the contents of one of the data storage registers to the burst configuration register depending on the slot type.

51. A method for recovering data symbols transmitted over a

cable system, the method comprising the steps of:

recovering from the cable system a data representative signal having symbols occurring at a given symbol rate;

sampling the signal at the given symbol rate; and

adjusting the phase of a symbol clock to match the symbols of the signal.

52. The method of claim 51, additionally comprising the step of converting the recovered signal to digital form before the sampling step.

53. The method of claim 52, additionally comprising the step of down-converting the recovered signal before the sampling step.

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